Improved Hierarchical Test Generation Technique for Combinational Circuits with Repetitive Sub-Circuits," IEEE Proc. Test Symp., pp. 237-243).

On page 6 of the Office Action, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §102(e) as being anticipated by Hachiya (U.S. Patent No. 6,031,979).

On pages 7-9 of the Office Action, the Examiner rejected claims 9-12, 14-24, 26-36, and 38-44 under 35 U.S.C. §103(a) as being unpatentable over Shinsha et al. (U.S. Patent No. 4,882,690); or Wang et al. ("Restructuring Binary Decision Diagrams Based on Functional Equivalence," IEEE Design Automation, pp. 261-65); or Kuehlmann et al. ("Equivalence Checking Using Cuts and Heaps," IEEE Proc. 1997 Design Auto. Conf., pp. 263-68).

The Present Invention

Claim 9 of the present invention specifies that a plurality of partial circuits are extracted from a circuit to be simulated, and that the partial circuits exhibiting equivalent operational characteristics are integrated into one partial circuit before the circuit is simulated. Independent claims 21 and 33 recite similar language.

The Filseth Reference

The Filseth reference discloses a method for flattening hierarchical descriptions of electronic circuits by using a program called a "linker" or "flattener," which is included in modern electronic computer-aided design (ECAD) tools (Filseth at col. 1, line 12 to col. 2 line 15).

In Filseth, logic circuit descriptions represented hierarchically must be expanded into flat circuit descriptions to perform circuit simulation for complex logic circuits. The program "linker" or "flattener" is used in Filseth merely to expand logic circuit descriptions represented hierarchically into flat circuit descriptions to perform circuit simulation for complex logic circuits.

In Filseth, the program "linker" or "flattener" reads hierarchical descriptions of logic circuits and produces flat circuit descriptions that are enlarged in circuit size more than the hierarchical descriptions, on the presumption that the hierarchical descriptions of logic circuits cannot be used to perform circuit simulation, and that circuit simulation can be performed only by using flat logic circuits represented by the enlarged flat circuit descriptions. Consequently,

the time required to perform circuit simulation in Filseth using flat logic circuits increases substantially due to an enlargement of circuit size in the flat logic circuits.

In contrast, in the present invention, circuit simulation is performed using a circuit that has been compressed by integrating partial circuits exhibiting equivalent operational characteristics into one partial circuit. Thus, in the present invention, the time required to perform circuit simulation can be reduced substantially because the circuit used for circuit simulation is reduced in circuit size by integrating partial circuits exhibiting equivalent operational characteristics into one partial circuit.

Thus, the method in Filseth for flattening hierarchical descriptions of logic circuits using the "linker" or "flattener" program is very different from the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Yokomizo Reference

Yokomizo discloses a circuit recognition and reduction method for pattern-based circuit simulation, in which circuit elements extracted from layout pattern data are combined together to recognize new circuit data, including logic gates, and the recognized circuit data are reduced by tracing signal flows and picking up the logic gates along the specified circuit paths.

Thus, the circuit recognition and reduction method of Yokomizo is quite different from circuit simulation of the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Chakrabarti Reference

The Chakrabarti reference discloses a hierarchical test generation technique for combinational circuits with repetitive sub-circuits, in which the regularity of one circuit is exploited by grouping together identical gate-level sub-circuits into high-level sub-circuits based upon the characteristics of logical operations. In contrast, in the present invention, a plurality of

partial circuits that are to be inspected for equivalence are extracted from a circuit based upon configurations of the plurality of partial circuits exhibiting equivalent operational characteristics.

Also, in Chakrabarti, test vectors are produced after grouping together identical gate-level sub-circuits into high-level sub-circuits. In contrast, in the present invention, circuit simulation is performed by integrating a plurality of partial circuits that are determined to exhibit equivalent operational characteristics into one partial circuit.

Thus, the hierarchical test generation technique of Chakrabarti differs from circuit simulation of the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Hachiya Reference

The Hachiya reference discloses a circuit patterning apparatus for executing parallel circuit simulation, in which a target circuit is partitioned into a plurality of clusters so that the update operation times are identical for every cluster prior to execution of circuit simulation.

Thus, the circuit patterning apparatus of Hachiya that executes parallel circuit simulation is very different from the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits, which are determined to exhibit equivalent operational characteristics, into one partial circuit.

The Shinsha Reference

The Shinsha reference discloses a method for automatically updating gate-level logic according to an alteration in functional-level logic.

In Shinsha, when new gate-level logic is produced by altering functional-level logic, the new gate-level logic that has been altered is compared with the current gate-level logic that has not been altered. Both corresponding portions (or sub-logics) that are common logically to the new gate-level logic and the current gate-level logic, and non-corresponding portions that are not common logically to the new gate-level logic and the current gate-level logic, are extracted to distinguish the corresponding portions from the non-corresponding portions. In other words,

it is determined in Shinsha whether there are any corresponding portions (or sub-logics) that are common to the new gate-level logic and the current gate-level logic, only on the basis of functional-level logic.

In contrast, in the present invention, it is determined whether partial circuits extracted from a circuit exhibit equivalent operational characteristics based upon configurations of these partial circuits, for example, component elements of these partial circuits and the connectional relationship between these component elements.

Therefore, Shinsha has a disadvantage in that it may be determined that two kinds of sub-logics having very different delay characteristics are common to each other. Even though two kinds of sub-logics may have the same functional-level logic, delay time of signals that are to be transferred in one sub-logic may be different from that in the other sub-logic if circuit configurations differ from each other. In contrast, in the present invention, it is possible to overcome the disadvantage of Shinsha because it is determined in the present invention whether partial circuits extracted from a circuit exhibit equivalent operational characteristics based upon configurations of these partial circuits.

Thus, the method of Shinsha for automatically updating gate-level logic is very different from the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits that are determined to exhibit equivalent operational characteristics into one partial circuit.

The Wang Reference

The Wang reference discloses a method for restructuring Binary Decision Diagrams (BDDs) from a given input ordering to any other ordering, based upon the concept of functional equivalence and structure equivalence of the BDDs.

Thus, the method of Wang for restructuring BDDs is very different from the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits that are determined to exhibit equivalent operational characteristics into one partial circuit.

The Kuehlmann Reference

The Kuehlmann reference discloses a method for comparing large combinational circuits with some structural similarities by using BDDs.

Thus, the method of Kuehlmann for comparing large combinational circuits with some structural similarities is very different from the present invention, in which circuit simulation is performed by integrating a plurality of partial circuits that are determined to exhibit equivalent operational characteristics into one partial circuit.

The Dependent Claims

As for the dependent claims, the dependent claims depend from the above-discussed independent claims and are patentable over the prior art for the reasons discussed above.

Therefore, Applicants submit that claims 9-12, 14-24, 26-36, and 38-44 patentably distinguish over the prior art. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejections under §§ 102 and 103.

Request for Examiner Interview Prior to Next Office Action

If the claims continue to be rejected after reconsideration of the claims, the Examiner is respectfully requested to contact the undersigned by telephone to arrange an Examiner Interview prior to issuance of the next Office Action.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding rejections, the application is submitted to be in condition for allowance, which action is earnestly solicited.

Finally, if there are any additional fees associated with filing of this response, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 10/29/02

By: C. Joan Gilsdorf
Christine Joan Gilsdorf
Registration No. 43,635

700 Eleventh Street, NW, Suite 500
Washington, D.C. 20001
(202) 434-1500

CERTIFICATE UNDER 37 CFR 1.8(a)

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on Oct. 29, 2002

STAAS & HALSEY

By: C. Joan Gilsdorf

Date: 10/29/02